

CLAIMS

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1. An electronic component comprising:
a substrate; and
an airbridge located over the substrate and having at least a first layer and a second layer
over the first layer,
wherein:
the airbridge is electrically conductive; and
the first layer of the airbridge is less resistive than the second layer of the airbridge.

2. The electronic component of claim 1 wherein:
the second layer is a passivation layer.

3. The electronic component of claim 1 wherein:
the second layer is harder than the first layer.

4. The electronic component of claim 1 wherein:
a gap exists between a portion of the airbridge and the substrate; and
a thickness of the second layer is less than a combined thickness of the first layer and the
gap.

5. The electronic component of claim 4 wherein:

1 the thickness of the second layer is less than fifty percent of the combined thickness of the first layer and the gap.

2 first layer and the gap.

3 *But A²*

4 the second layer is located underneath an edge of the first layer.

5 The electronic component of claim 1 wherein:

6 *1st / 1st*

7. The electronic component of claim 1 wherein:
the second layer is absent underneath a center portion of a width of the airbridge.

8. The electronic component of claim 1 wherein:
a gap exists underneath a portion of the airbridge; and
the gap is unsealed underneath the portion of the airbridge.

9. The electronic component of claim 1 wherein:
the second layer of the airbridge has a compressive stress level of approximately 0 to 200

12 MegaPascals.

10. The electronic component of claim 1 wherein:
the airbridge further comprises:
a third layer underneath the first layer; and
the third layer is more resistive than the first layer.

11. The electronic component of claim 10 wherein:

1 the second layer is more resistive than the third layer.

2 12. The electronic component of claim 1 wherein:

3 the second layer of the airbridge is electrically conductive.

4 13. The electronic component of claim 1 wherein:

5 the second layer of the airbridge is electrically insulative.

6 14. A semiconductor component comprising:

7 a semiconductor substrate;

8 a semiconductor device supported by the semiconductor substrate;

9 a first electrically insulative layer overlying the semiconductor substrate and the

10 semiconductor device; and

11 an airbridge located over the semiconductor substrate, located over the first electrically

12 insulative layer, and electrically coupled to the semiconductor device,

13 wherein:

14 the airbridge has a first electrically conductive layer; and

15 the airbridge has a second electrically insulative layer overlying the first electrically

16 conductive layer.

17 15. The semiconductor component of claim 14 wherein:

18 a gap exists between a portion of the airbridge and the first electrically insulative layer;

1 the second electrically insulative layer is a passivation layer harder than the first electrically
 2 conductive layer; and
 3 the airbridge further comprises:
 4 an electrically conductive barrier layer located underneath the first electrically
 5 conductive layer and more resistive than the first electrically conductive layer.

6 16. The semiconductor component of claim 15 wherein:
 7 a thickness of the second electrically insulative layer is less than fifty percent of a
 8 combined thickness of the electrically conductive barrier layer, the first electrically conductive
 9 layer, and the gap.
 10 17. The semiconductor component of claim 15 wherein:

11 the second electrically insulative layer is devoid of sealing the gap underneath the portion
 12 of the airbridge.

13 18. The semiconductor component of claim 14 wherein:

14 the second electrically insulative layer is absent underneath a center portion of a width of
 15 the airbridge.

16 19. The semiconductor component of claim 14 wherein:

17 the second electrically insulative layer has a compressive stress level of approximately 100
 18 MegaPascals.

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1 ✓ 20. A method of manufacturing an electronic component comprising:
2 providing a substrate;
3 forming a first layer over the substrate to form a first portion of an airbridge; and
4 forming a second layer over the first layer to form a second portion of the airbridge over
5 the substrate,
6 wherein:
7 the airbridge is electrically conductive; and
8 the first layer of the airbridge is less resistive than the second layer of the airbridge.

9 21. The method of claim 20 further comprising:
10 forming a semiconductor device at least partially located within the substrate; and
11 forming an electrically insulative layer over the substrate and the semiconductor device,
12 wherein:
13 forming the first layer further comprises:
14 providing the first layer comprised of an electrically conductive material;
15 and
16 forming the second layer further comprises:
17 providing the second layer comprised of an electrically insulative material.

18 22. The method of claim 20 further comprising:
19 forming a semiconductor device at least partially located within the substrate;
20 forming an electrically insulative layer over the substrate and the semiconductor device;
21 and

1 forming a sacrificial layer over a portion of the substrate before forming the first layer
2 comprising:
3 reflowing the sacrificial layer; and
4 baking the sacrificial layer.

5 23. The method of claim 22 wherein:

6 forming the sacrificial layer further comprises:

7 providing photoresist for the sacrificial layer; and

8 developing the sacrificial layer before reflowing the sacrificial layer.

9 24. The method of claim 23 wherein:

10 forming the sacrificial layer further comprises:

11 avoiding exposing the sacrificial layer to deep ultra violet light after developing the
12 sacrificial layer.

13 25. The method of claim 22 wherein:

14 reflowing the sacrificial layer further comprises:

15 ramping a reflow temperature from a first temperature up to a second temperature
16 during a first period of time;

17 heating the sacrificial layer from the first temperature up to the second temperature
18 during the first period of time; and

19 heating the sacrificial layer at the second temperature during a second period of
20 time; and

1 baking the sacrificial layer further comprises:
2 ramping a baking temperature from a third temperature up to a fourth temperature
3 during a third period of time;
4 heating the sacrificial layer from the third temperature up to the fourth temperature
5 during the third period of time; and
6 heating the sacrificial layer at the fourth temperature during a fourth period of
7 time.

8 26. The method of claim 25 wherein:
9 baking the sacrificial layer further comprises:
10 providing the third temperature equal to the second temperature.

11 27. The method of claim 22 further comprising:
12 removing the sacrificial layer after forming the first layer.

13 28. The method of claim 22 further comprising:
14 removing the sacrificial layer before forming the second layer.

15 29. The method of claim 22 wherein:
16 forming the second layer further comprises:
17 depositing the second layer;
18 disposing a photoresist layer over the second layer;
19 baking the photoresist layer over a range of temperatures;

1 exposing the photoresist layer to actinic radiation;
2 developing the photoresist layer;
3 etching the second layer; and
4 removing the photoresist layer after etching the second layer.

5 30. The method of claim 29 wherein:

6 baking the photoresist layer further comprises:

7 heating the photoresist layer over the range of temperatures during a first time
8 period.

9 31. The method of claim 29 wherein

10 forming the second layer further comprises

11 avoiding exposing the photoresist layer to deep ultra violet light after developing
12 the photoresist layer; and

13 avoiding exposing the photoresist layer to a baking process after developing the
14 photoresist layer.

15 32. The method of claim 29 further comprising:

16 using the photoresist layer to directly protect portions of the second layer, the first layer,
17 and the electrically insulative layer.

18 33. The method of claim 29 wherein:

19 baking the photoresist layer occurs only before exposing the photoresist layer.

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- 1 ✓ 34. The method of claim 20 further comprising:
2 designing the airbridge to have a design width,
3 wherein:
4 forming the first layer further comprises:
5 forming the first layer to have a first layer width greater than the design
6 width; and
7 forming the second layer further comprises:
8 forming a portion of the second layer underneath edges of the first layer;
9 and
10 keeping the second layer absent underneath a central portion of the first
11 layer, the central portion of the first layer having the design width.